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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,831	07/01/2003	Antonio Maria Borneo	851763.435	3911

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EXAMINER	
TECKLU, ISAAC TUKU	

ART UNIT	PAPER NUMBER
2192	

DATE MAILED: 08/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/612,831	BORNEO ET AL.	
	Examiner	Art Unit	
	Isaac T. Tecklu	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/01/03, 10/28/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the application filed on 07/01/2003.

2. Claims 1- 25 have been examined.

Oath/Declaration

3. The office acknowledges receipt of a properly signed oath/declaration filed on 01/29/2004.

Drawings

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: e.g. Fig. 8, element 100 and 102. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claims 13 and 14, recite acronym "VLIW", such acronym should be spelled out once in the claims as its intended meaning and utility are likely will be changed over the time. Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Odani et al. (US 6,367,067 B1).

As per claim 1, Odani discloses process for executing programs on a multiprocessor system having a plurality of processors, having a given instruction set architecture (e.g. Fig. 1, element 102 and related text), each of said processors being able to execute, at each processing cycle, a respective maximum number of instructions (e.g. Fig. 1 and related text), characterized in that it comprises the operations of:

compiling, at least in part, the instructions of said programs as instruction words of given length executable on a first processor of said plurality (in column 20 , lines 41-50 "... during compiling ... an instruction is inserted ..." and Fig. 9 and related text); and

modifying at least some of said instruction words of given length converting them into modified-instruction words executable on a second processor of said plurality (in column 5, lines 13-30 "... cross compiler ... divided constants ... reconstruct the original constant and the constructed constant ..."), said modification operation in turn having at least one operation selected from the group of:

splitting said instruction words into modified-instruction words (e.g. Fig. 11A-11C and related text); and

entering in the modified-instruction words no-operation instructions (in column 14, lines 45-50 a no-operation instruction is inserted ...").

As per claim 2, Odani discloses the process according to claim 1, characterized in that it comprises the operations of:

compiling the instructions of said programs in part as first instruction words having a first given length and executable on said first processor of said plurality and in part as second instruction words of given length executable on a second processor of said plurality (in column 20 , lines 41-50 "... during compiling ... an instruction is inserted ..." and Fig. 9 and related text);

modifying at least some of said first instruction words into first modified-instruction words executable on said second processor of said plurality (in column 5, lines 23-30 "... translating source code written in a high language ..."); and

modifying at least some of said second instruction words into second modified-instruction words executable on said first processor of said plurality (e.g. Fig. 5, element 16 and 46 and related text).

As per claim 3, Odani discloses the process according to claim 2, characterized in that said first instruction words and said second instruction words have, respectively, a first and a second maximum length with said first maximum length greater than said second maximum length (in column 3, lines 15-23 ".. when the final size is greater than the assumed size..."), the quotient between said first maximum length and said second maximum length having a given value with the possible presence of a remainder (in column 8, lines 45-50 "... divided constant ..." and Fig. 5, element 12 and related text)and in that the procedure comprises the operations of:

modifying said first instruction words by having said first maximum length into first modified-instruction words having said second maximum length by (in column 8, lines 45-50 "... short constant ..."):

splitting said first instruction words into a number of said first modified-instruction words equal to the value of said quotient (e.g. Fig. 11A-11C and related text); and

in the presence of said remainder, adding to said first modified-instruction words a further modified-instruction word of length equal to said second maximum length, said second maximum length being obtained by entering into said further first modified-instruction word a set of no-operation instructions; and

modifying said second instruction words by having said second maximum length into second modified-instruction words having said first maximum length by:

adding to said second instruction words of said second maximum length a number of no-operation instructions equal to the difference between said first maximum length and said second maximum length (in column 14, lines 45-50 a no-operation instruction is inserted ...").

As per claim 4, Odani discloses the process according to claim 1 characterized in that it comprises the operations of:

encoding said instructions on a given number of bits, said number of bits having a first bit identifying a length of instruction word executable on a processor of said plurality (e.g. Fig. 20A –20C and related text);

associating to said given number of bits a respective appendix having a set of further bits identifying lengths of instruction words executable on different processors of said plurality (e.g. Fig. 17A-G and related text);

identifying for each of said instructions a processor of said plurality designed to execute said instruction, said identified processor being able to process for each processing cycle a given length of instruction word (in column 3, lines 15-21 "... size determination step ..." and in column 8, lines 63-67 "... when the size of label can be determined ..."); and

entering in the position of said first identifier bit a chosen bit between said further bits of said appendix, said chosen bit identifying the length of instruction word that can be executed by said identified processor (in column 8, lines 63-67 and in column 9, lines 1-5 "... the size is added to the label as size ...").

As per claim 5, Odani discloses the process according to claim 4, characterized in that it comprises the operation of erasing said respective appendix before execution of the instruction (in column 12, lines 22-30 "... deleting one instruction from the group ...").

As per claim 6, Odani discloses the process according to claim 4, characterized in that said chosen bit is entered in the position of said first identifier bit in a step chosen from among: decoding of the instruction in view of the execution (e.g. Fig. 1, element 103-105 and related text); re-filling of the cache associated to said identified processor (e.g. Fig. 1, element 106 and related text); and decompression of the instruction in view of the execution (in column 12, lines 50-55 "... code size being reduced ...").

As per claim 7, Odani discloses the process according to claim 1, characterized in that it comprises the operation of:

alternatively distributing the execution of the instructions of said sequence between the processors of said plurality, said instructions being directly executable by the processors of said plurality in conditions of binary compatibility (e.g. Fig. 1, element 100 Processor, element 106 and related text).

As per claim 8, Odani discloses the process according to claim 1, characterized in that it comprises the operation of selectively distributing the execution of said instructions among the processors of said plurality, distributing dynamically the computational load of said processors (e.g. Fig. 1, element 100 Processor, element 106 and related text).

As per claim 9, Odani discloses the process according to claim 1, characterized in that it comprises the operation of selectively distributing the execution of said instructions between said processors of said plurality with the criterion of equalizing the operating frequency of the processors of said plurality (e.g. Fig. 1, element 107 and related text).

As per claim 10, Odani discloses the process according to claim 1, characterized in that it comprises the operation of performing a control process executed by at least one of the

processors of said plurality so as to equalize its own workload with respect to the other processors of said multiprocessor system (e.g. Fig. 5, element 12 and related text).

As per claim 11, Odani discloses the process according to claim 1, characterized in that it comprises the operation of drawing up a table accessible by said control process, said table having items selected from the group of:

a list of processes being executed or suspended on any processor of said plurality of processors (in column 18, lines 20-25 "... terminates it relocation ...");

the progressive number thereof according to the order of activation; the percentage of maximum power of the processor that is used by said process (in column 23, lines 50-55 "... maximum address size of the target processor..");

the execution time, said time, if zero, indicating that the process is temporarily suspended from being executed (in column 18, lines 20-25 "... terminates ...");

the amount of memory of the system used by the process to be able to execute the function for which it is responsible (in column 23, lines 50-55 "... most common size ...");

the maximum length of the long instruction that the VLIW processor can execute and for which it had been generated during compiling (in column 23, lines 50-55 "... maximum address size of the target processor...");

maximum length of the long instruction of the VLIW processor on which it is executed (in column 16, lines 50-60 "... possible number of instruction executed ..."); and

the address of the portion of memory in which the data and the instructions are stored (Fig. 5, element 17 Linker Unit).

As per claim 12, this multiprocessor version of the claimed process discussed above (Claim 1), wherein all claim limitations have been addressed and/or covered in cited areas as set forth above. Thus, accordingly, these claims are also anticipated by Odani.

As per claim 13, Odani discloses the multiprocessor system according to claim 12, characterized in that said processors are all of the VLIW type (e.g. Fig. 1, element 100, VLIW).

As per claim 14, Odani discloses the multiprocessor system according to claim 12, characterized in that said plurality of processors comprises at least one VLIW processor and at least one superscalar processor (e.g. Fig. 1, Address, VLIW).

As per claim 15, Odani discloses a system comprising:

a plurality of processors coupled for receiving instruction sets (e.g. Fig. 1, element 100 and 102 and related text);

a first processor of the plurality coupled to each of the other processors within said plurality, said first processor receiving from the other processors data representative of the workload of each of said other processors (e.g. Fig. 1 and related text);

an output signal from said first processor to said instruction set stream, said output signal controlling the instructions, which are sent to each of said processors based on the results of the workload measurement of said processors (e.g. Fig. 1, element 106 and related text).

As per claim 16, Odani discloses the system according to claim 15, wherein said workload measurement comprises power consumption of each of said processors of said plurality (in column 23, lines 50-55 "... maximum address size of the target processor...").

As per claim 17, Odani discloses the system according to claim 15, wherein said workload measurement comprises memory usage of each of said processors of said plurality (in column 23, lines 50-55 "... maximum address size of the target processor...").

As per claim 18, Odani discloses the system according to claim 15, wherein said workload measurement comprises number of operations carried out by each of said processors of said plurality (in column 23, lines 50-55 "... maximum address size of the target processor...").

As per claim 19, Odani discloses a process of directing instruction sets to be executed by a plurality of processors in a system comprising:

receiving a plurality of instruction sets on a bus line connected to said processors (e.g. Fig. 1, element 100 and related text);

receiving workload data at a first processor of said plurality of processors (e.g. Fig. 1, element 100 and related text), said workload data being representative of workload of each of the processors of said plurality (e.g. Fig. 1, element 102 and 105 and related text);

comparing the workload of each of the processors (e.g. Fig. 9, element 23 INSTRUCTION INSERTION UNIT); and

sending a signal from said first processor based on the data representative of the workload of each of the processors of said plurality to the bus line for modifying the number of instruction sets sent to each processor based on their respective workloads (e.g. Fig. 9, element 24 and related text).

As per claim 20, Odani discloses the process according to claim 19, wherein said workload data includes data regarding power consumption of each of said processors of said plurality (in column 23, lines 50-55 "... maximum address size of the target processor...").

As per claim 21, Odani discloses he system according to claim 19, wherein said workload data includes data regarding memory usage of each of said processors of said plurality (in column 23, lines 50-55 "... maximum address size of the target processor...").

As per claim 22, Odani discloses the system according to claim 19, wherein said workload data includes data regarding the number of operations carried out by each of said processors of
said plurality (in column 16, lines 50-60 "... possible number of instruction executed ...").

As per claim 23, Odani discloses a process for executing programs in a system having a plurality of processors comprising:

receiving instructions of said programs, a first set of said instructions having a first word length, and second set of said instructions having a second word length (e.g. Fig. 1, element 100 and related text), said first word length being longer than said second word length (e.g. Fig. 11A, element 400, 401 and 402 and related text);

modifying the length of said second instruction words by combining two or more of said second instruction words into one instruction word, the words selected for combining being selected to ensure that the length of the combined instruction word does not exceed said first word length (in column 5, lines 23-30 "... translating source code written in a high language ...");

adding no-operation instructions equal to the difference between said first word length and the combined instruction word length to said combined instruction word (in column 14, lines 45-50 a no-operation instruction is inserted ...").

As per claim 24, Odani discloses the process according to claim 23, wherein said first word length is equal to an exact multiple of said second word length, such that the combined instruction word equals the first word length and no no-operation instructions are added (e.g. Fig. 8, element S44 and S45 and related text).

As per claim 25, Odani discloses the process according to claim 23, wherein said instructions are further modified comprising: encoding said instructions on a given number of bits, said number of bits having a first bit identifying the number of no-operation instructions within the instruction word (e.g. Fig. 20A –20C and related text).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Isaac T. Tecklu whose telephone number is (571) 272-7957. The examiner can normally be reached on M-TH 9:300A - 8:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Examiner
Issac Tecklu
Art Unit 2192

TUAN DAM
SUPERVISORY PATENT EXAMINER